Rayhan Etwaree

rayhan.etwaree@gmail.com | GitHub |Linkedin|Personal Website

Professional Experience

AI Trainer (Aether Generalist) – Outlier Dec 2025 - Jan 2026

Remote | Freelance

- Evaluated, ranked and optimized AI-generated prompts and queries
- Applied strong grammatical and logical knowledge when assessing model output
- Identified errors in generated content
- Performed tasks for different projects with high accuracy in a fast-paced environment

Education

Toronto Metropolitan University – B.E. in Computer Engineering Expected May 2028

Relevant Coursework – Object-Oriented Analysis and Design, Engineering Algorithms and Data Structures, Digital Systems, Electronic Circuits

Skills

Programming Languages: Java, C, C++, VHDL, MATLAB

Frameworks & Tools: Git/GitHub, Quartus II, MPLAB x IDE, Multisim

Electronics: RTL Design, FPGA Altera DE2 board, Op-Amps, Oscilloscope, Multimeter, ESP32

Projects

FPGA-Based 8-bit General Purpose Processor Github

- Designed and implemented an 8-bit microprocessor on a Cyclone II FPGA
- Developed VHDL modules for the ALU, 4-to-16 microcode decoder, register file and FSM-based control unit, and seven-segment display interface
- Implemented an ALU supporting arithmetic, logic and bitwise operations, including addition, subtraction and parity evaluation
- Validated all modules using Quartus II waveform analysis

Digital Oscilloscope & Waveform Generator Github|Demonstration

- Designed and programmed a mixed-signal testing device in C++ capable of generating AC waveforms
- Leveraged the ESP32's internal Digital-to-Analog Converter to synthesize a smooth sine wave, using a potentiometer input to map and scale the signals amplitude

Battleship Remake Github

- Developed a Java-based Battleship game with a Swing graphical user interface supporting player versus AI gameplay
- Implemented an AI targeting algorithm that prioritized adjacent cells after successful hits
- Applied object-oriented design principles to improve modularity, readability, and maintainability of the codebase

4-Bit Adder Subtractor Unit Github

- Implemented a full adder and two's complement logic to handle both addition and subtraction on an FPGA
- Created a modular architecture in VHDL with separate entities for arithmetic logic and seven-segment display
- Integrated negative sign display logic for the seven-segment output
- Built a waveform testbench for debugging

Leadership/Extracurriculars

1241 First Robotics Team Member – Mississauga, Ontario September 2023 – June 2024

- Assisted in creating a robot that qualified for the FRC World Championship, placing in the top 10 during the Ontario 2024 season
- Supported electrical and mechanical design, fabrication, and assembly of a competition-ready robot
- Mentored students during LEGO Mindstorms workshops, teaching programming, design and robotics concepts